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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,786	02/24/2004	Hasan Nejad	M4065.0509/P509 B	2218

24998 7590 06/27/2005

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EXAMINER	
NGUYEN, VIET Q	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 06/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H-A

Office Action Summary	Application No.	Applicant(s)	
	10/784,786	NEJAD ET AL.	
	Examiner	Art Unit	
	Viet Q. Nguyen	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *THREE* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Amendment filed on 5/5/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *34-36 and 62-73* is/are pending in the application.

4a) Of the above claim(s) *34-36 and 70-73* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *62-69* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/5/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on **5/5/2005** has been entered and made of record.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims **62-29** are rejected under 35 U.S.C. 102(e) as being anticipated by **Seyyedy (US 6,754,124).**

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Seyyedy et al (se Fig. 1) teaches a memory device comprising a plurality of slices (or layers, planes, etc.) of MRAM cells (38). Fig.2 also shows that each such slice

or layer also comprising an array of such cells arranged in rows and columns (44, 39) and having an associated access transistor (16), see col. 2-4.

Regarding the claimed steps of a method for reading such memory cells, Seyyedy et al teaches the following:

- Fig. 2, both row decoder (81) and column decoder (82) are used to perform the "decoding an address associated with a selected cell in a particular slice/plane by determining the a row address and a layer address of particular slice',

- Col. 5 (lines 24-43) mentions the use of a read/write common line where reading/writing voltage can be applied for selecting an associated address',

- Col. 5 (lines 24-43) mentions the use of sense amplifier for sensing a logic state of selected cell at such associated address by activating the access transistor',

- Col. 5 (lines 24-43) mentions the sensing step performed by determining the resistance level of such selected memory cell;

- Col. 5 (lines 24-43) mentions the reading step performed by determining the X-axis direction and Y-Z plane direction through decodes (81, 82) as claimed.

Regarding claims 71-73, col. 6 (lines 20-29) mentions the use of line (31a, Fig. 3) as a reference line for holding a reference voltage level so that the resistance of selected cell can be compared using the sense amp (50).

Regarding the claimed "sense interconnect line", col. 5 (lines 9-15) mentions the sense line interconnected (32), which is itself electrically connected to the access transistor (16).

Regarding the claimed "resistive" memory as pure resistance material for representing a logic state of the memory cell (as claimed by the instant application), it should be understood that Seyyedy et al invention is not certainly limited to the ***MRAM*** type only because his invention has already suggested other use and/or other memory type materials. Particularly, see columns 7-8, mentions that "... while the invention has been described within the context of memory devices employing MRAM cells, ***other types of memory cells such as programmable conductor RAM*** (***PCRAM***) cells may also be used with the present invention." However, because ***PCRAM*** is well-known in the art as a type of "***resistive***" memory (which employs conductive materials) where its conductor material also has its resistance varied according to program voltage applied to its conductor and/or the programmed logic state of the memory cell, one having ordinary skilled in the art can see that ***PCRAM*** or any other similar resistive memory cell type, if any, is inherent disclosed and/or already suggested for use by this Seyyedy invention too.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Viet Q. Nguyen whose telephone number is (571) 272-1788. The examiner can normally be reached on 7am-6pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Viet Q Nguyen
Primary Examiner
Art Unit 2827

V. Nguyen
6/19/2005